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(71) Applicant: TRIMBLE NAVIGATION LIMITED [US/US]; 645 North Mary Avenue, Sunnyvale, CA 94086 (US).

(72) Inventors: LAU, Chung, Y.; 859 Russet Drive, Sunnyvale, CA 94087 (US). PARKER, Reed, A.; 19660 Junipero Way, Saratoga, CA 95027 (US). RODAL, Eric, B.; 18615 Castle Lake Drive, Morgan Hills, CA 95037 (US).

(74) Agents: GALLENSON, Mavis, S. et al.; Ladas & Parry, Suite 2100, 5670 Wilshire Boulevard, Los Angeles, CA 90036 (US).

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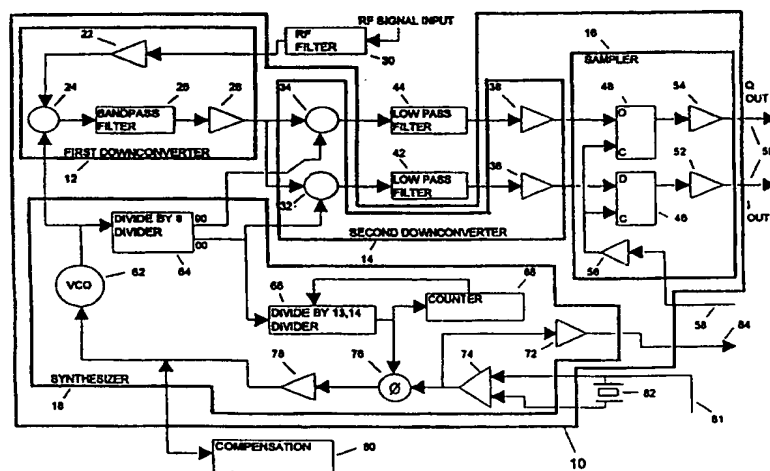
(57) Abstract

A GPS/GSM receiver combination for receiving GSM and GPS signals using an RF GPS integrated circuit for downconverting the GPS signal. The GPS integrated circuit includes a synthesizer for generating LO signals, first and second downconverters for using the LO signals, and a sampler for providing in–phase and quadrature phase sampled output signals representative of the GPS signal. The synthesizer includes a multi–mode divider for providing substantially the same first LO frequency at about the midpoint of the L1 and L2 GPS frequencies when either of a standard GSM reference frequency or historically common GPS reference frequency is selected. A standby mode in the integrated circuit is controlled by a power logic circuit using a power supply input as a logic control signal. The GSM/GPS receiver combination includes a GSM reference oscillator and a microprocessor system including a GSM frequency correction code for correcting the GSM reference frequency based upon a frequency correction beacon (FCB) signal received in the GSM frequency. The GSM–based correction is then used for correcting the GSM reference frequency in order to center a frequency search for acquiring the GPS signal.

GSM CELLULAR TELEPHONE AND GPS RECEIVER COMBINATION

5   BACKGROUND OF THE INVENTION

Field of the Invention

        The invention relates generally to cellular
10 telephones and more particularly to a Global System for
Mobile telecommunications cellular telephone and global
positioning system (GSM/GPS) receiver combination using a
single chip RF integrated circuit having an efficient
divider scheme for using either of a GSM standard
15 reference frequency or a second reference frequency for
downconverting a GPS signal.

Description of the Prior Art

20   Global Positioning System (GPS) receivers determine
location, velocity, and time by receiving and processing
information in GPS signals received from GPS satellites
that have been placed in orbit around the Earth by the
United States Government. The GPS signal from each
25 satellite carries data for the location-in-space of the
satellite and time-of-transmission on carrier frequencies
that are the same for all the satellites. The data from
each satellite is spread with a pseudo-random noise (prn)
code that is distinct for that satellite. A GPS receiver
30 uses the distinct prn code for distinguishing the GPS
signals from typically at least four satellites and then
finds its own location, velocity, and time by solving
simultaneous equations using the relative times that the
signal from each of the satellites arrives at the
35 receiver and the locations-in-space and times-of-
transmission from the satellites.

There is a continuous need for improving the
performance of GPS receivers in terms of accuracy,
acquisition and tracking of low level signals,
acquisition time, and immunity to interference. And,
5   there is a continuous need for reducing the size, power
consumption, and cost of the GPS receiver. One of the
major components in determining the performance, size,
power, and cost in the GPS receiver is the radio
frequency (RF) circuitry at the front end for
10   downconverting the GPS satellite carrier frequency to an
intermediate or baseband frequency. A second major
component is the digital signal processor (DSP) circuitry
for processing the signal at the intermediate or baseband
frequency for providing GPS signal correlations. Due to
15   the relatively high frequency of the GPS satellite
signal, most GPS receivers until recently have used
discrete components for the front end RF circuitry.
Although the performance of such RF circuitry may be very
good, these discrete components represent a large portion
20   of the size, power, and cost of a modern GPS receiver.
Gallium Arsenide (GaAs) integrated circuits (IC)s have
been developed using field effect transistors (FET)s as
active devices for replacing the majority of the discrete
components in the RF circuitry. Unfortunately, GaAs ICs
25   have been and continue to be relatively expensive because
the commercial manufacturing volume of GaAs ICs is low
and because the GaAs material is more expensive than
Silicon and the processing steps in manufacturing a GaAs
IC are relatively difficult. Silicon bipolar ICs using
30   bipolar transistors as active devices have been used for
the front end RF circuitry in the GPS receiver. Such ICs
can be more difficult to design because the frequency
response, noise figure, and power consumption for the
silicon IC bipolar transistors are typically not as good
35   as for the GaAs IC FETs. However, the silicon bipolar ICs
are less costly and have recently been shown to have

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sufficient performance for most applications. There
continues to be a need for improvements in RF ICs in
order to improve performance and reduce size, power
consumption, and cost in a GPS receiver.

5   Cellular telephones are commonly used together with
GPS receivers for communicating the location of the
receiver. In most of these uses the location is read by
a human user from a stand alone GPS receiver and then
spoken into a stand alone cellular telephone. In an
10 improvement over this system, the location is
communicated electronically from the GPS receiver to the
cellular telephone using a digital interface. Recently,
GPS receivers and cellular telephones have been packaged
together for reducing their combined cost and size by
15 sharing the same housing and power supply. However, in
existing systems where a GPS receiver and a cellular
telephone coexist in the same package they share little
functionality and little or nothing has been done to take
advantage of the circuitry and functions of the cellular
20 telephone for improving the performance and reducing the
cost of the GPS receiver. There is a need for a GPS
receiver and cellular telephone combination that uses
circuitry of the cellular telephone for improving the
performance and reducing the cost of the GPS receiver.

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SUMMARY OF THE INVENTION

It is therefore an object of the present invention
to provide a global system for mobile telecommunications
cellular telephone and global positioning system
(GSM/GPS) receiver combination using a GSM signal for
correcting the frequency of an internal reference signal
for reducing the GPS signal acquisition time of the GPS
receiver.

Another object of a GSM/GPS receiver combination of
the present invention is to share a GSM reference
oscillator by a GSM receiver and a GPS receiver.

Another object of the present invention is to
provide a single radio frequency (RF) GPS integrated
circuit (IC) for downconverting either an L1 or an L2 GPS
signal using either a standard GSM reference frequency or
a historically common GPS reference frequency as a
frequency reference.

Briefly, in a preferred embodiment, a GPS RF
integrated circuit (IC) of the present invention includes
a synthesizer for providing a first local oscillator (LO)
signal and a complex second LO signal, a first
downconverter using the first LO signal for converting a
GPS L1 or L2 frequency signal to a first intermediate
frequency (IF) signal, a second downconverter using the
second LO signal for converting the first IF signal to a
complex second IF signal, and a sampler using a clock
signal received from a GPS DSP IC for sampling the second
IF signal and issuing I and Q sampled signals. Either
the L1 frequency or the L2 frequency is selected in an RF
filter before the GPS signal reaches the GPS RF IC. The
frequency of the first LO signal is at about the mid-
point of the L1 and L2 frequencies so that the first and
second intermediate frequencies are substantially equal
for receiving the L1 or L2 frequencies by using mixing

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products for frequency differences where the incoming GPS
signal is higher or lower, respectively, than the
frequency of the LO signal. The synthesizer includes an
amplifier/oscillator for selectably receiving an external

5   reference signal at a standard GSM reference frequency of
about thirteen megahertz or generating an internal
reference signal using an external resonator at a
historically common GPS reference frequency about twelve
and one-half megahertz; and a multi-mode divider for

10   frequency dividing the second LO signal by a first or a
second divide number so that the first and second LO
frequencies do not change significantly when the
reference frequency is changed. The first divide number
is a ratio formed by alternating two integer divide

15   numbers in repeating sequences.
        A GSM/GPS receiver combination of the present
invention includes a GSM reference oscillator; a GSM
cellular telephone receiver; a GPS receiver including the
GPS DSP IC and a GPS RF section including the RF GPS IC;

20   a power supply; and a microprocessor system. The GSM
reference oscillator provides a GSM reference signal for
the external reference signal to the GPS RF IC. The GPS
RF IC then issues the GSM reference signal to the GPS DSP
IC and the GSM receiver. The GSM receiver receives a GSM

25   signal including communication information and a
frequency correction beacon (FCB) signal including a
frequency having a frequency standard accuracy and
provides the microprocessor system with information for a
frequency difference between the frequency of the GSM

30   reference signal and the frequency that the GSM reference
signal would be if it were derived from the same
frequency standard as the FCB signal. The GSM-based
frequency difference is passed from the GSM receiver to
the microprocessor system.

35   The GPS receiver receives the GPS signal including
location-determination information and passes GPS

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correlation signals to the microprocessor system. The
microprocessor system uses the correlation signals for
determining when the GPS signal has been acquired and,
after the GPS signal has been acquired, for determining
5   location, velocity, and time. In order to acquire the
GPS signal the microprocessor system calculates an
expected frequency offset for correcting a frequency
difference between the frequency of the reference signal
that has been selected and the frequency that it would be
10 if were derived from the same frequency standard as the
GPS signal. The GPS DSP IC uses the expected frequency
offset for offsetting the reference frequency and then
uses the offset reference frequency as the basis for
generating a replica signal. The replica signal is
15 correlated with the GPS signal for providing correlation
signals that indicate when the GPS signal has been
acquired. When the GPS signal cannot be acquired with
the expected frequency offset, the microprocessor system
increments or decrements the expected frequency offset in
20 a search pattern until the GPS signal is acquired. In
the present invention the microprocessor system includes
a frequency correction code using the GSM-based frequency
difference for improving the accuracy of the expected
frequency offset for the GSM reference frequency.
25 Because both the FCB signal and the GPS signal are
typically derived from atomic standards, the use of the
GSM-based frequency difference reduces or eliminates the
number of increments and decrements to the frequency
offset that must be searched in order to acquire the GPS
30 signal thereby reducing the time required to acquire the
GPS signal.

An advantage of a GSM/GPS receiver combination of
the present invention is that GPS signal acquisition time
is reduced (improved) by using a GSM signal including a
35 frequency correction beacon (FCB) signal for correcting

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the accuracy of a locally generated GSM reference
frequency.

      Another advantage of the present invention is that a
GSM reference oscillator is shared by a GSM receiver and
5   a GPS receiver, thereby reducing the cost of a GSM/GPS
receiver combination of the present invention.

      Another advantage of the present invention is that a
single RF GPS integrated circuit can use historically
common reference frequencies for either GSM or GPS for
10   downconverting an L1 or L2 GPS signal, thereby increasing
its volume and the applications in which it can be used
without modification.

      These and other objects and advantages of the
present invention will no doubt become obvious to those
15   of ordinary skill in the art after having read the
following detailed description of the preferred
embodiments which are illustrated in the various figures.

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IN THE DRAWINGS

Fig. 1 is a block diagram of a RF GPS integrated circuit downconverter of the present invention; and

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Fig. 2 is a block diagram of a GSM cellular telephone receiver and GPS receiver combination of the present invention using the integrated circuit of Fig. 1.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 illustrates a radio frequency (RF) integrated circuit of the present invention referred to by the
5 general reference number 10 for receiving a global positioning system (GPS) signal. The integrated circuit 10 includes a first downconverter 12, a second downconverter 14, a sampler 16, and a synthesizer 18. The first downconverter 12 includes a low noise amplifier
10 (LNA) 22, a mixer 24, a low pass filter 26, and an amplifier 28 for receiving a radio frequency input signal. Typically, the RF signal passes through an RF filter 30 before reaching the integrated circuit 10. The LNA 22 receives an RF input signal from outside the
15 integrated circuit 10 and passes an amplified RF signal to the mixer 24. The mixer 24 uses a first local oscillator (LO$_1$) signal received from the synthesizer 18 to downconvert the frequency of the amplified RF signal and passes the downconverted signal to the low pass
20 filter 26. The low pass filter 26 filters the downconverted signal and passes a filtered signal to the amplifier 28. The amplifier 28 amplifies the filtered signal and passes the amplified signal as a first intermediate frequency (IF) signal the second
25 downconverter 14.

The second downconverter 14 includes a pair of mixers 32 and 34 and a pair of amplifiers 36 and 38. The first IF signal is split and passed to each of the mixers 32 and 34. The mixer 32 uses an in-phase (I) component
30 of a complex second local oscillator (LO$_2$) signal received from the synthesizer 18 to downconvert the first IF signal to an I channel second IF signal; and the mixer 34 uses a quadrature (Q) component of the complex LO$_2$ signal received from the synthesizer 18 to downconvert the first
35 IF signal to a Q channel second IF signal. The I and Q channels of the complex second IF signal are passed off

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chip through low pass filters 42 and 44 and received back
on chip to the amplifiers 36 and 38. The amplifiers 36
and 38 amplify the signals and pass the I and Q signals
to the sampler 16.

5   The sampler 16 includes a pair of D flip-flops 46
and 48, a pair of output amplifiers 52 and 54, and a
clock input amplifier 56. The clock input amplifier 56
amplifies a sampling clock input signal from a path 58
and passes the amplified clock signal to clock inputs (C)
10   of the D flip-flops 46 and 48. The D flip-flops 46 and
48 receive the I and Q second IF signal components at D
inputs and use an edge of the amplified clock signal for
providing sampled I and Q output signals, respectively.
The sampled I and Q signals are amplified by the output
15   amplifiers 52 and 54 and then passed out of the
integrated circuit 10 as I and Q output signals to a path
59.

          The synthesizer 18 includes a voltage controlled
oscillator 62, a divide-by-eight divider 64, a divide-by-
20   thirteen, fourteen divider 66, a counter 68, a clock
output amplifier 72, a reference amplifier/oscillator 74,
a phase detector ($\emptyset$) 76, and an error voltage amplifier
78. The divide-by-eight divider 64 uses a divide-by-two
divider followed by a divide-by-four Johnson counter to
25   establish a fixed 90° phase offset between two divide-by-
four outputs. The VCO 62, the divider 64, the divider
66, the phase detector 76, the error voltage amplifier
78, and an off
chip compensation circuit 80 act as a phase lock loop to
30   synchronize the frequency of the LO_1 and LO_2 signals to a
reference signal from a path 81 having a reference
frequency of either thirteen megahertz or twelve point
five zero four (12.504) megahertz. The VCO 62 generates
the LO_1 signal having a frequency controlled by an
35   amplified error voltage signal provided by the error
voltage amplifier 78. The LO_1 signal is frequency divided

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by eight by the divider 64 and split into the LO$_2$ I (0°)
and Q(90°) components used in the second downconverter 14.
The LO$_2$ I component is frequency divided by either
thirteen or fourteen in the divider 66 as controlled by a
5   divide selection signal from the counter 68. The divider
66 then passes a frequency divided feedback signal to the
counter 68 and the phase detector 76.

The reference amplifier/oscillator 74 uses positive
feedback around a differential amplifier for generating
10   the reference signal or uses the differential amplifier
for amplifying an externally generated reference signal.
For operation as an oscillator, a crystal resonator 82
having a desired resonant frequency is connected between
two emitter coupled inputs to the amplifier/oscillator
15   74. For operation as an amplifier the inputs of the
amplifier/oscillator 74 receive the externally generated
reference signal from the path 81. The reference
amplifier/oscillator 74 passes the reference signal to
the phase detector 76. The phase detector 76 provides an
20   error voltage proportional to a difference in phases
between the amplified reference signal and the feedback
signal received from the divider 66 The compensation
circuit uses a capacitor or a combination of one or more
capacitors and/or resistors for frequency stability by
25   adding the appropriate poles and zeros for stabilizing
the loop. The clock output amplifier 72 receives the
reference signal from the reference amplifier/oscillator
74 and issues a reference signal output to a path 84.

The integrated circuit 10 has a first mode using the
30   thirteen megahertz reference frequency and a second mode
using the twelve point five zero four megahertz reference
frequency. The feedback signal provided by the divider
66 is a pulse stream having an average pulse rate that is
driven by the action of the loop to match the frequency
35   of the reference signal. The divide select signal
provided by the counter 68 causes the divider 66 to·

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divide by thirteen or by fourteen. In the first mode the
counter 68 counts the frequency divided signal from the
divider 66 to fifteen and provides a divide select signal
causing the divider 66 to frequency divide the LO_2

5   frequency in repeating sequences of 13, 14, 13, 14, 13,
14, 13, 14, 13, 14, 13, 14, 13, 14, and 13. The average
divide number in the divider 66 is found by dividing the
sum of thirteen times eight plus fourteen times seven by
the sum of eight plus seven. Equation 1 below shows the

10   average divide number in a general form.

Divide number = $(A_N * A_t + B_N * B_t) / (A_t + B_t)$ (1

In a preferred embodiment of the generalized

15   equation 1, A_N is thirteen, A_t is eight, B_N is fourteen,
and B_t is seven, the average divide number equals two-
hundred two divided by fifteen (202/15) or thirteen point
four followed by sixes (13.466666). Accordingly, in the
first mode, the LO_2 signal has a nominal frequency of

20   about 175.067 megahertz and the LO_1 signal has a nominal
frequency of about 1400.533 megahertz. In the second
mode the counter 68 provides the divide selection signal
having the second logic level thereby controlling the
divider 66 to divide by fourteen. Accordingly, in the

25   second mode LO_2 signal has a nominal frequency of 175.056
megahertz and the LO_1 signal has a nominal frequency of
1400.448 megahertz. For an L1 GPS frequency of 1575.42
megahertz, the first downconverted signal has a center
frequency of approximately 174.887 megahertz or 174.972

30   megahertz for the first and second modes, respectively;
and the second downconverted signal has a center
frequency of approximately 180 kilohertz or 84 kilohertz
for the first and second modes, respectively. For an L2
GPS frequency of 1227.60 megahertz, the first

35   downconverted signal has a center frequency of
approximately 172.933 megahertz or 172.848 megahertz for

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the first and second modes, respectively, and the second
downconverted signal has a center frequency of about 2.13
megahertz or about 2.21 megahertz in the first and second
modes, respectively. Importantly, the center frequencies
5   of the first IF signals for the L1 and L2 GPS frequencies
for either reference frequency are close enough to enable
the integrated circuit 10 to use a single low pass filter
26 and the second IF frequency is low enough for the
sampled signals to be inexpensively processed by a
10 following digital processor. It will be appreciated that
the above scheme is not limited to an average divide
number of two-hundred two divided by fifteen or for
reference frequencies of only thirteen and twelve point
five zero four megahertz. The sampling clock input
15 signal on the path 58 has a frequency that is equal or
harmonically related to the reference frequency. In
preferred a embodiment the frequency of the sampling
clock input is ¼ of the reference frequency or 3.25
megahertz or 3.126 megahertz for the preferred first or
20 second modes, respectively.

       Fig. 2 illustrates a global system for mobile
telecommunication cellular and global positioning system
(GSM/GPS) receiver combination of the present invention
25 referred to by the general reference number 100. The
GSM/GPS receiver 100 includes a GSM reference generator
102; a GSM antenna 112; a GSM receiver 113 including a
GSM RF section 114 and a GSM digital signal processor
(DSP) section 116; a microprocessor system 120, a GPS
30 antenna 122; a GPS receiver 123 including a GPS DSP IC
124 and associated circuitry and a GPS RF section 130,
and a power supply 131. The GSM reference generator 102
provides a GSM reference signal to the GPS RF section 130
on the path 81 at the standard GSM reference frequency of
35 thirteen megahertz. The GPS RF section 130 includes the
integrated circuit 10, the RF filter 30, the low pass

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filters 42 and 44, the compensation 80, and the crystal resonator 82 all of which are illustrated in Fig. 1 and described in the accompanying detailed description. The GPS RF section 130 selects the GSM reference signal or

5   generates the reference signal using the resonator 82 and then distributes the selected reference signal through the path 84 to the GSM RF section 114, the GSM DSP section 116, and the GPS DSP IC 124; thereby eliminating the requirement of having a separate reference clock

10   generator for each of the GSM circuitry and the GPS circuitry. The GPS DSP IC 124 passes the reference signal from the path 84 back to the GPS RF section 130 through the path 58 or divides the frequency of the reference signal by a number such as four and returns the

15   divided signal back to the GPS RF section 130 through the path 58 as the sampling clock input signal.

The GSM antenna 112 receives an airwave RF signal transmitted according to the GSM cellular standard and passes a representative conducted GSM RF signal to the

20   GSM RF section 114. The GSM RF section 114 frequency downconverts the RF signal and passes the information in the signal to the GSM DSP section 116 at a lower frequency. The GSM DSP section 116 processes the information according to instructions received from the

25   microprocessor system 120 through a signal bus 132 having address and data, and outputs voice information through a speaker 134. In the other direction, a microphone 136 passes voice information to the GSM DSP section 116 which is passed in a low frequency signal to the GSM RF section

30   114 and to the GSM antenna 112 for transmission.

The GPS antenna 122 receives a GPS RF signal and passes the signal to the GPS RF section 130. The GPS RF section 130 downconverts the RF signal to representative I and Q low frequency signals as described above and

35   passes the I and Q signals through the path 59 and the reference signal through the path 84 to the GPS DSP IC

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124. The GPS DSP IC 124 cooperates with the
microprocessor system 120 over the bus 132 to acquire and
track the GPS signal by generating a replica signal and
correlating and synchronizing the replica signal to the
5   sampled (I) and (Q) signals. While the GPS signal is
being tracked, the GPS DSP IC 124 passes correlation
signals including GPS location-determination information
for the health and locations-in-space, phase
observations, and Doppler frequencies of the GPS
10   satellites over the bus 132 to the microprocessor system
120. Details of the downconversion and correlation of
the GPS signal are described in United States Patent No.
4,672,629 entitled "Receiver for Bandspread Signals" by
Beier and United States Patent No. 5,402,347 entitled
15   "Satellite Search Methods For Improving Time To First Fix
In A GPS Receiver" by McBurney et al. The teachings of
these patents are incorporated herein by reference. The
microprocessor system 120 then uses the GPS information
for calculating the location and velocity of the GPS
20   antenna 122 and time. The processed information for
location, velocity, and/or time is then passed to a
display 142 for visual presentation, through a path 144
as a serial digital output, and/or to the GSM DSP section
116 for output through the GSM RF section 114 and GSM
25   antenna 112. A user enters requests to the
microprocessor system 120 through a keypad 146 or in a
serial digital input through the path 144. The
microprocessor system 120 includes a memory including a
pre-programmed code for processing the requests and
30   controlling the elements of the GSM/GPS receiver 100.
     The GSM RF receiver 113 has a standby mode
controlled by pre-programmed code in the microprocessor
system 120 for reducing power consumption when no GSM
communication is being transmitted or received. The GSM
35   cellular signal includes a frequency correction beacon
(FCB) signal having a known precise frequency offset of

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fifty-seven kilohertz from its carrier typically derived
from an atomic clock. During the standby mode, the GSM
receiver 113 periodically compares the reference
frequency to the frequency of the FCB signal and provides
5   information for a measured reference frequency using the
frequency of the FCB signal as the standard to the
microprocessor system 120 over the bus 132. The
microprocessor system 120 includes a pre-programmed
executable GSM frequency correction code 150 for
10   directing the GSM receiver 113 for measuring the
reference frequency and calculating a reference frequency
correction based upon a difference between the measured
reference frequency and the known frequency of the FCB
signal. The frequency correction is then used along with
15   other information such as the expected Doppler frequency
offsets for the GPS satellites for calculating an
expected frequency offset for the reference frequency and
providing information for the expected offset to the GPS
DSP IC 124 over the bus 132. The GPS DSP IC 124 then
20   uses the expected frequency offset for adjusting the
reference frequency to an initial center frequency that
is used for generating a replica signal for correlating
to the GPS signal and passes correlation signals over the
bus 132 to the microprocessor system 120. When the
25   correlation exceeds a correlation threshold the GPS
signal is considered to have been acquired and continuing
information in the correlation signals is used by the
microprocessor system 120 for determining location and
velocity of the GPS antenna 122 and time. If, after
30   following a preprogrammed acquisition procedure, the
correlation threshold is not exceeded, the microprocessor
system 120 searches for the frequency of the GPS signal
by incrementing and/or decrementing the frequency offset
and follows acquisition procedure again. Because the
35   center frequency used initially is transferred from the
more accurate frequency of the FCB signal, the range of

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frequencies that must be searched is reduced, thereby
decreasing the time for acquiring the GPS signal.
Further details of the GPS acquisition procedure are
disclosed in the U. S. Patent No. 5,402,347 by McBurney
5   incorporated herein by reference.

Although the present invention has been described in
terms of the presently preferred embodiments, it is to be
understood that such disclosure is not to be interpreted
10   as limiting. Various alterations and modifications will
no doubt become apparent to those skilled in the art
after having read the above disclosure. Accordingly, it
is intended that the appended claims be interpreted as
covering all alterations and modifications as fall within
15   the true spirit and scope of the invention.
        What is claimed is:

CLAIMS

1. A GSM/GPS receiver combination for receiving a global system for mobile telecommunications (GSM) signal including information for a GSM communication and a global positioning system (GPS) signal including information for a GPS location, comprising:

a GSM reference oscillator for providing a GSM reference signal having a standard GSM reference frequency;

a GSM receiver for using said GSM reference signal for receiving said GSM signal and providing said GSM communication;

a GPS receiver for using said GSM reference signal for receiving said GPS signal and providing a GPS correlation signal; and

a microprocessor system for cooperating with the GPS receiver for processing said GPS correlation signal for providing said GPS location.

2. The receiver combination of claim 1, wherein:

said GSM signal further includes a GSM frequency correction beacon (FCB) signal;

the GPS receiver includes a GPS digital signal processing (DSP) section for receiving said GSM reference signal; and

the microprocessor system includes a GSM frequency correction code for directing the GSM receiver for using a frequency of said FCB signal for measuring said GSM reference frequency, using said GSM reference frequency measurement for calculating a GSM-based frequency correction to said GSM reference frequency, and providing said GSM-based frequency correction to said GPS DSP section for

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correcting said GSM reference frequency for acquiring said
GPS signal.

3.   The receiver combination of claim 2, wherein:
        said GPS DSP section is for using said GSM
reference frequency and said GSM-based frequency correction
for centering a frequency search for acquiring said GPS
signal.

4.   The receiver combination of claim 1, wherein:
        said standard GSM reference frequency is about
thirteen megahertz.

5.   The receiver combination of claim 1, wherein:
        the GPS receiver includes an amplifier/oscillator
for selecting a reference signal of one of (i) said GSM
reference signal or (ii) a second reference signal having a
second reference frequency not equal to said GSM reference
frequency and using said selected reference signal for
receiving said GPS signal and providing said GPS correlation.
signal.

6.   The receiver combination of claim 5, wherein:
        the GPS receiver includes a synthesizer for
generating a local oscillator (LO) signal from said selected
reference signal, said LO signal having substantially the
same frequency for either of (i) said GSM reference signal
and (ii) said second reference signal; a downconverter using
said LO signal for downconverting said GPS signal and
providing a downconverter output signal; and a GPS digital
signal processor (DSP) for using said downconverter output

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signal and said selected reference signal for providing said GPS correlation signal.

7.   The receiver combination of claim 6, wherein:
            said LO signal has a frequency approximately the midpoint of an L1 frequency and an L2 frequency of said GPS signal.

8.   The receiver combination of claim 6, wherein:
            said synthesizer includes a phase detector coupled to the amplifier/oscillator for receiving said selected reference signal and providing an error signal corresponding to a phase difference between said selected reference signal and a feedback signal; a local oscillator for providing said LO signal having an LO frequency corresponding to said error signal; and a multi-mode divider for frequency dividing said LO signal by a selected one of a first divide number for providing said feedback signal having said GSM reference frequency or a second divide number for providing said feedback signal having said second reference frequency.

9.   The receiver combination of claim 8, wherein:
            at least one of said first divide number and said second divide number has an average of a ratio having an integer numerator and an integer denominator, said denominator greater than one.

10.   The receiver combination of claim 8, wherein:
            said multi-mode divider is further for providing said average divide number by alternating a divide number A_N and a divide number B_N in repeating sequences, each of said

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sequences beginning in said divide number A_N and ending in said divide number A_N for providing said feedback signal.

11.   The receiver combination of claim 10, wherein:
        at least one of said first divide number and said second divide number is an integer number.

12.   The receiver combination of claim 6, wherein:
        said LO signal includes a first LO signal and a complex second LO signal at a sub-multiple of said first LO signal; and
        said downconverter includes a first downconverter for using said first LO signal for providing a first intermediate frequency (IF) signal, a second downconverter for using said second LO signal for providing a complex second IF signal, and a sampler for sampling said second IF signal for providing said downconverter output signal having in-phase (I) and quadrature phase (Q) components.

13.   A method for receiving a global system for mobile telecommunications (GSM) signal including information for a GSM communication and a global positioning system (GPS) signal including information for a GPS location in a GSM/GPS receiver combination, comprising steps of:
        generating a GSM reference signal having a standard GSM reference frequency;
        using said GSM reference signal for receiving said GSM signal and providing said GSM communication information;
        using said GSM reference signal for receiving said GPS signal and providing a GPS correlation signal; and
        processing said GPS correlation signal for providing said GPS location.

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14.   The method of claim 13, wherein:

said GSM signal further includes a GSM frequency correction beacon (FCB) signal; and further including steps of:

comparing said GSM reference frequency to a frequency of said FCB signal for providing a GSM-based frequency correction; and

using said GSM-based frequency correction for correcting said GSM reference frequency for acquiring said GPS signal.

15.   The method of claim 14, wherein:

said step of acquiring said GPS signal includes using said GSM reference frequency and said GSM-based frequency correction for centering a frequency search for said GPS signal.

16.   The method of claim 13, wherein:

said standard GSM reference frequency is about thirteen megahertz.

17.   The method of claim 13, further including steps of:

selecting a reference signal of one of (i) said GSM reference signal or (ii) a second reference signal having a second reference frequency not equal to said GSM reference frequency; and wherein:

the step of receiving said GPS signal includes using said selected reference signal for receiving said GPS signal and providing said GPS correlation signal.

18.   The method of claim 17, wherein:

the step of receiving said GPS signal further
includes steps of: generating a local oscillator (LO)
signal from said selected reference signal, said LO signal
having substantially the same frequency for either of (i)
said GSM reference signal and (ii) said second reference
signal; using said LO signal for downconverting said GPS
signal and deriving said GPS correlation signal from said
downconverted signal.

19. The method of claim 18, wherein:
        said LO signal has a frequency approximately the
midpoint of an L1 frequency and an L2 frequency of said GPS
signal.

20. The method of claim 18, wherein:
        said step of generating said LO signal includes
steps of phase comparing said selected reference signal to a
feedback signal for providing an error signal; using said
error signal for generating said LO signal; and frequency
dividing said LO signal by a selected one of a first divide
number for providing said feedback signal having said GSM
standard reference frequency or a second divide number for
providing said feedback signal having said second reference
frequency.

21. The method of claim 20, wherein:
        at least one of said first divide number and said
second divide number has an average of a ratio having an
integer numerator and an integer denominator, said
denominator greater than one.

22. The method of claim 21, wherein:

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said step of frequency dividing said LO signal includes a step of frequency dividing by alternating a divide number A_N and a divide number B_N in repeating sequences where each of said sequences begins in said divide number A_N and ends in said divide number A_N.

23. The method of claim 22, wherein:

at least one of said first divide number and said second divide number is an integer number.

24. The method of claim 18, wherein:

said LO signal includes a first LO signal and a complex second LO signal at a sub-multiple of said first LO signal; and

said step of downconverting said GPS signal includes steps of: using said first LO signal for providing a first intermediate frequency (IF) signal; using said second LO signal for providing a complex second IF signal; and sampling said second IF signal for providing said downconverter output signal having in-phase (I) and quadrature phase (Q) components.

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Fig. 1

GSM CELLULAR
SIGNAL

GPS
SIGNAL

112

122

123

GSM
REFERENCE
GENERATOR
102

81

RF FILTER
30

LOW PASS
FILTERS
42 & 44

82

INTEGRATED
CIRCUIT   10

GSM
RF
SECTION

114

113

COMPENSATION
80

GPS RF
SECTION
130

84

58

59

GSM
DSP
SECTION
116

GPS
DSP
IC
124

POWER
SUPPLY
131

132

SPEAKER
134

MICROPROCESSOR
SYSTEM   120

DISPLAY
142

MICROPHONE
136

GSM FREQUENCY   150
CORRECTION CODE

KEYPAD
146

144

INPUT/OUTPUT
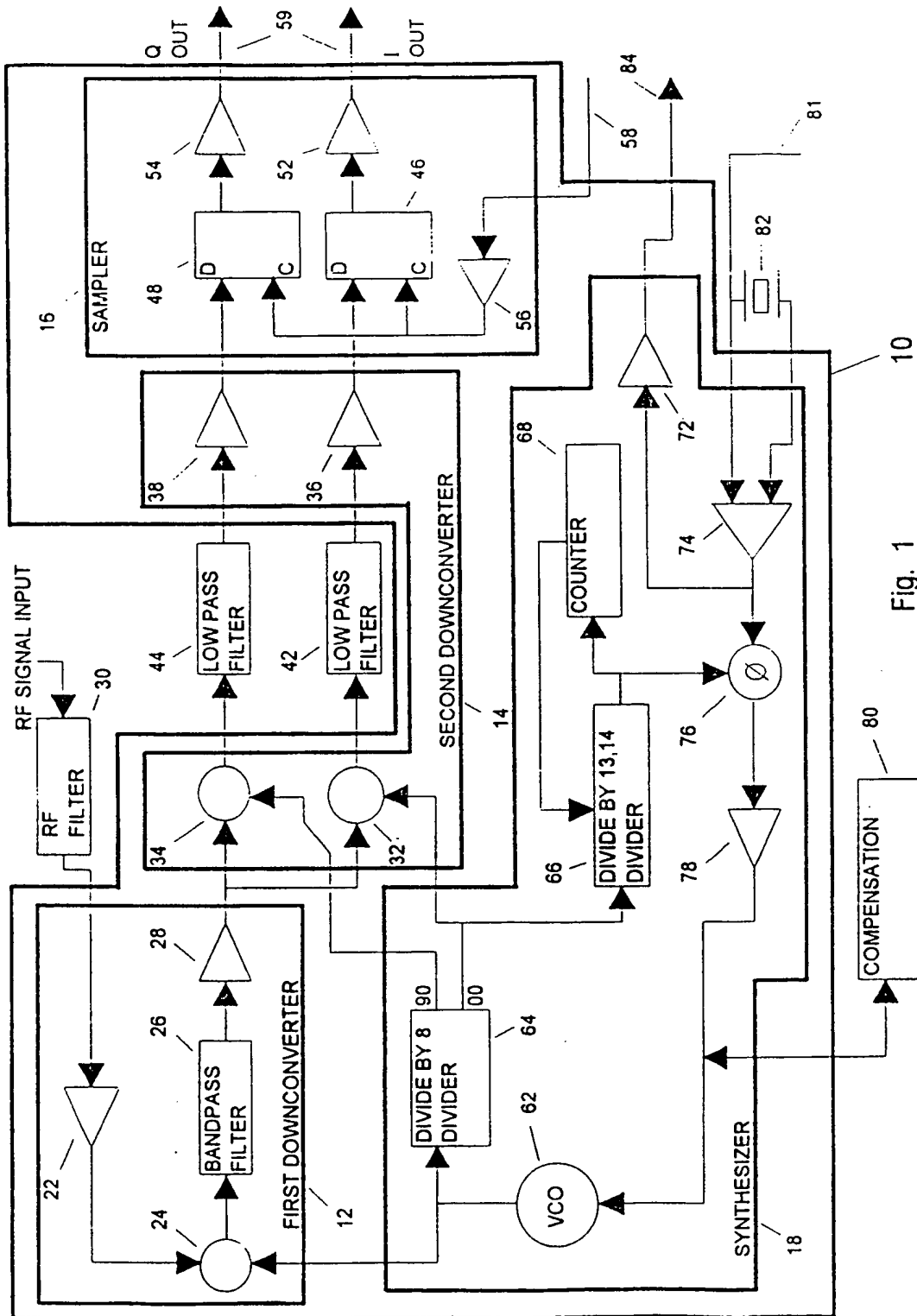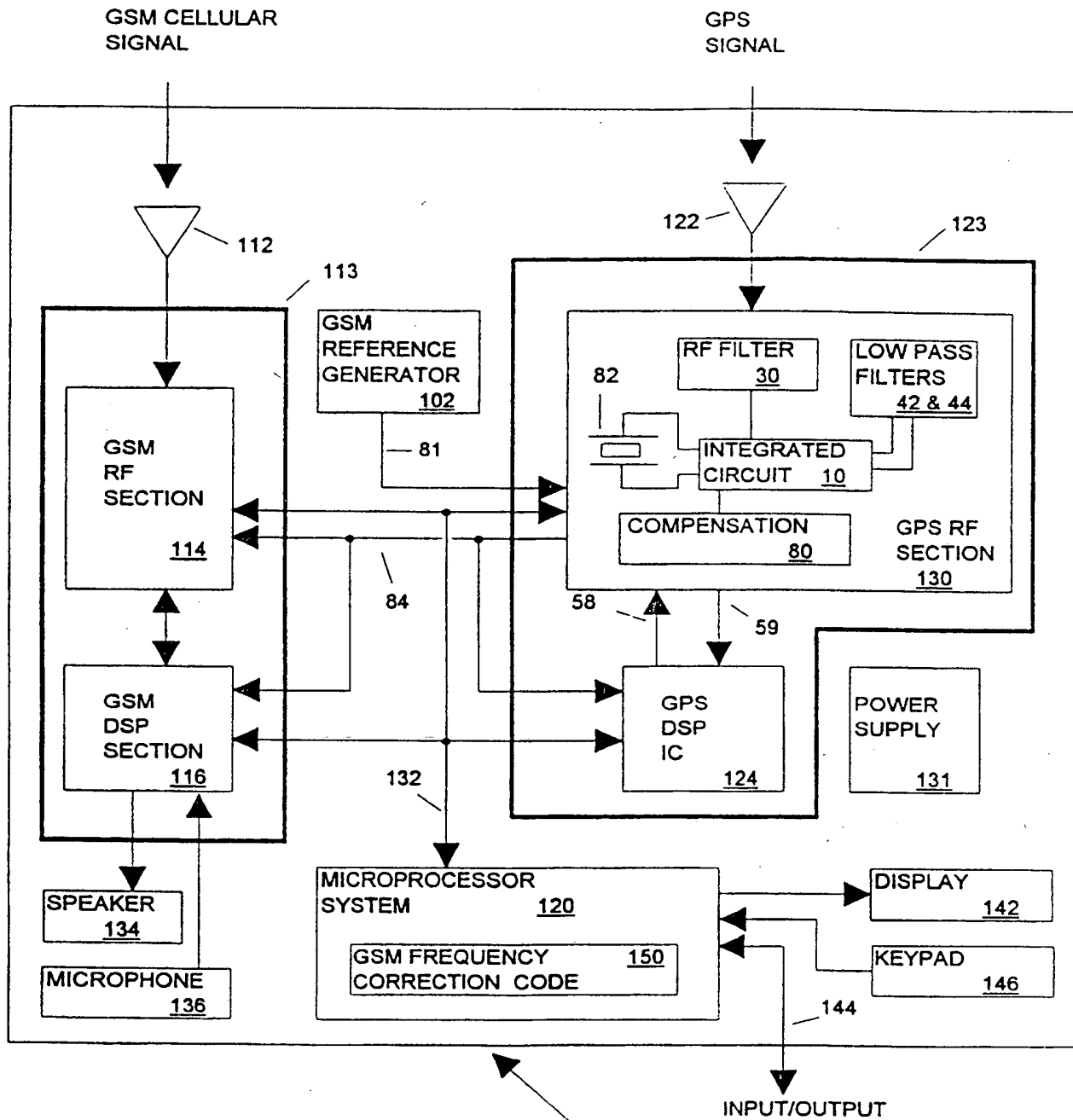
Fig. 2   100

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6   H04Q7/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6   H04Q   H04B   G01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	WO 99 13595 A (ERICSSON) 18 March 1999 (1999-03-18) abstract; figures 1,3-5,7,13 page 12, line 13 - page 13, line 2 page 15, line 3 - line 16 ---	1,13
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[X] Further documents are listed in the continuation of box C.   [X] Patent family members are listed in annex.

° Special categories of cited documents :

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 July 1999	23/07/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Danielidis, S

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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